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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,861	05/24/2000	Timothy J. Williams	0325.00339	4837

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	6

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/577,861	WILLIAMS, TIMOTHY J.	
	Examiner	Art Unit	
	Albert Wang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is responsive to Amendment B filed October 29, 2003. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-19, 22, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borras, U.S. Patent No. 5,128,938, in view of Philips Semiconductors, "74HC/HCT5555 Programmable delay timer with oscillator", September 1993 ("Philips").

As per claim 1, Borras teaches an apparatus comprising:

a first circuit configured to present a wake-up signal in response to an input signal (Fig. 2, timer 202 presents wake-up signal via line 242 in response to an input signal via line 236); and

a second circuit (Fig. 2, microcontroller 206) configured (i) to exit a suspend or sleep mode in response to said wake-up signal (Col. 5, lines 16-24) and (ii) to generate said input signal, wherein said input signal comprises a programmable delay value (Fig. 3, step 302; Col. 4, line 66 – Col. 5, line 10).

However, Borras does not expressly teach details of the first circuit such as presenting any of a plurality of divided delay signals as a wake-up signal. Philips teaches a first circuit that presents any of a plurality of divided delay signals as a wake-up signal (Figs. 3 & 4, 24-stage

counter; Page 2, divide-by range of 2 to 2^{24}). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the details of Philips' first circuit to Borras's apparatus. A motivation for doing so would have been to ensure the integrity of the first circuit.

As per claims 2 and 3, Philips teaches a timer input signal comprising a programmable multi-bit signal (Fig. 3, inputs S_0 to S_3).

As per claim 4, Borras teaches said programmable delay value is determined in response to one or more firmware instructions (Col. 4, line 66 – Col. 5, line 10).

As per claim 5, Borras teaches a wake-up delay timing value (Fig. 3, step 302).

As per claim 6, Philips teaches said first circuit comprises:

a delay circuit configured to generate a delay signal (Page 4, first paragraph); and

a select circuit configured to (i) generate said plurality of divided delay signals and (ii) and present said wake-up signal in response to said delay signal and said input signal (Fig. 4).

As per claim 7, Philips teaches said input signal is configured to control selection of one of said plurality of divided delay signals for presentation as said wake-up signal (Fig. 4).

As per claim 8, Philips teaches each of said divided delay signals has a period that comprises a multiple of a period of said delay signal (Page 2, divide-by range of 2 to 2^{24}; Page 4, "counter divides the frequency to obtain a long pulse duration").

As per claim 9, Philips teaches said select circuit is configured to multiplex said plurality of divided delay signals in response to said input signal (Fig. 4).

As per claim 10, Philips teaches said select circuit comprises:

a divider circuit configured to generate said plurality of divided delay signals in response to said delay signal (Fig. 4); and

a multiplexer configured to present said wake-up signal in response to said plurality of divided delay signals and said input signal (Fig. 4).

As per claim 11, Philips teaches said first circuit comprises a counter configured to generate each of said plurality of divided delay signals in response to a different value of said input signal (Fig. 4).

As per claim 12, Philips teaches said delay circuit is further configured to present said delay signal in response to an enable signal (Fig. 3, trigger inputs A or B).

As per claim 13, Borras teaches said input signal is generated in response to a value stored in a register of said second circuit (Col. 4, line 66 – Col. 5, line 10).

As per claim 22, Borras teaches said first circuit is configured to periodically wake up said second circuit and a sleep period of said second circuit is determined by said programmable delay value (Fig. 3).

As per claim 14, Borras teaches a apparatus comprising:

a first circuit configured to operate in a sleep mode and a wake-up mode (Fig. 2, microcontroller 206; Col. 5, lines 16-24); and

a second circuit configured to control switching of said first circuit from said sleep mode to said wake-up mode after a programmable period of time (Fig. 2 timer 202; Fig. 3, step 302). However, Borras does not expressly teach details of the second circuit. Philips teaches a second circuit that comprises:

(i) a delay block configured to generate a delay signal in response to an enable signal (Fig. 3, oscillator configuration generates delay in response to trigger inputs A or B) and

(ii) a divider circuit configured to generate a plurality of divided delay signals in response to said delay signal (Fig. 3, 24-stage counter), where said divided delay signals determined a range of said programmable period of time (Page 2, divide-by range of 2 to 2^{24}).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the details of Philips' second circuit to Borras's apparatus. A motivation for doing so would have been to ensure the integrity of the second circuit.

As per claim 25, Philips teaches said second circuit is configured to determine said programmable period of time in response to an input signal comprising a programmable delay value (Fig. 3, inputs S_0 to S_3).

As per claims 15-19, since Borras/Philips teaches the apparatus of claims 1-14, 22, and 25, the combination teaches the claimed method.

3. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borras/Philips as applied to claim 1 above, and further in view of Yach et al., U.S. Patent No. 5,454,114 ("Yach").

As per claim 21, Borras/Philips is silent with regards to implementing said first and second circuits on a single integrated circuit. Yach teaches a single integrated circuit comprising first and second circuits (Fig. 1, microcontroller chip 10). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Yach's implementation of a single integrated chip to Borras/Philips' apparatus. A motivation for doing so would have been to take advantage of device integration (Yach, Col. 1, lines 48-66).

4. Claims 20, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borras/Philips as applied to claims 1 and 15 above, and further in view of Lee et al., U.S. Patent No. 6,025,745 ("Lee").

As per claims 20, 23 and 24, Borras/Philips does not expressly teach calibrating a programmable delay circuit. Lee teaches the steps for calibrating a delay circuit (Fig. 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to Lee's calibrating to Borras/Philips' method in order to adjust delay to account for variations such as those due to variations in environment and manufacture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
December 23, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100